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Linear Convolution with UT Vedic Multiplier using VHDL

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Abstract

Linear Convolution is one of the elemental operations of Signal processing systems and is used by some Multiplication Algorithms. In this project, the Linear Convolution is performed using ancient Multiplication Algorithm called Urdhva Triyagbhyam (UT) which is one among the 16 sutras in Vedic mathematics. This provides best results in speed when compared to other multipliers. Urdhva Triyagbhyam technique is used to increase the timing performance of the design. It is aimed to design the 8 bit convolution using UT. From various multiplication techniques, Urdhva- Tiryagbhyam sutra is being implemented because this sutra is applicable to all cases of algorithms for NxN bit numbers and the minimum delay is obtained. A 4x4 Vedic Multiplier design using special Adders which is having reduced delay is proposed. Then 8-bit multiplier is designed using four 4-bit multiplier and three Adders. The 8x8 Vedic Multiplier is used for Convolution. The low power and area efficient Modified Carry Select Adder (MCSLA) makes the system to a more efficient one. This is coded in VHDL, synthesized and simulated using Xilinx ISE Software.

Keywords:- Linear Convolution, Modified Carry Select Adder (MCSLA), Vedic Multiplier design.

Introduction

Convolution is the mathematical way of combining two signals to obtain a new signal. This is the operation used in signal processing application to predict the impulse response of a system. Linear Convolution is preferred for finite length sequences of any length. The process of convolution solely depends upon the multiplication process which is performed using Vedic multiplier of Ancient Indian Vedic Mathematics to enhance the computational speed of the system. The functional block has been simulated in Xilinks and implemented for Spartan 6 Field Programmable Gate Array (FPGA).

Motivation

The reason for focusing on the area of Convolution is that, it has found various applications on

fields like Digital Signal Processing (DSP), Digital Image Processing (DIP), Linear Acoustics and Statistics. Three signals play a vital role in order to perform convolution i.e., the input signal (x[n]), the output signal (y[n]), and the impulse response (h[n]). It finds its significance in the fields of Fourier Theory, analysis of linear systems and it is fundamental to many common image processing operators. Impulse function is mainly used for convolution in discrete cases. In linear time invariant systems, a product of input and impulse signals known as convolution. The product of the two signals, stick to the commutative property of algebra. It provides a way of "multiplying together" two arrays of numbers of different sizes with the same dimensionality, to produce a third array of numbers without the change in the dimensionality. While considering two sequences m(x) and h(x), where m(x) is the input sequence, h(x) is the impulse response. The output response of the system g(x) is computed as follows:

g(x) = m(x) * h(x) Where * represents convolution.

FPGA design is preferred as it employs very fast inputs, outputs (IOs) and bidirectional data buses which are used to verify correct time of valid data. Vedic Multiplier is comparatively faster than conventional multipliers.

Convolution

The most widely used types of Convolution are Linear and Circular. Linear Convolution is preferred for finite length sequences. The convolution of f and g is composed f * g, utilizing a reference mark or star. It is characterized as the basic of the result of the two functions after one is turned around and moved[2].

The basic steps involved in performing linear convolution are as follows :

Step 1: Consider two length of sequences l and m for x(n) and h(n) respectively.

Step 2: The total length of the output sequence is computed as **n = l + m - 1**.

Step 3:The output sequence y(n) is given by

$$\mathbf{y(n)} = \Sigma\, \mathbf{x(k)\, h(n-k)} \text{ (K varies from } -\infty \text{ to } \infty)$$

Step 4: Multiply the two sequences x(k) and h(n-k) element by element and sum up the products to get y(n).

Step 5: Increment the index n, shift the sequence h(n-k) to right by one sample and perform the 4th step.

Step 6: Repeat step 5 until the sum of products is zero for all the remaining values of n.

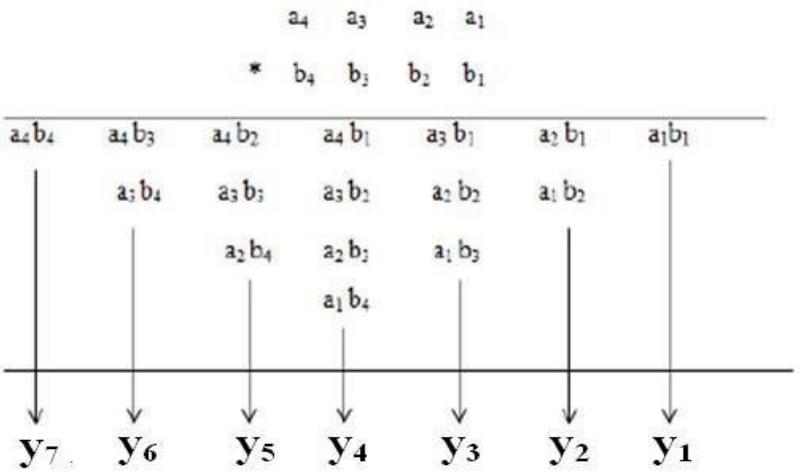

Figure 1: Convolution of two sequences

If the Length of x(n) is 4, and Length of h(n) is 4,

Length of y(n) = 4 + 4 - 1 = 7.

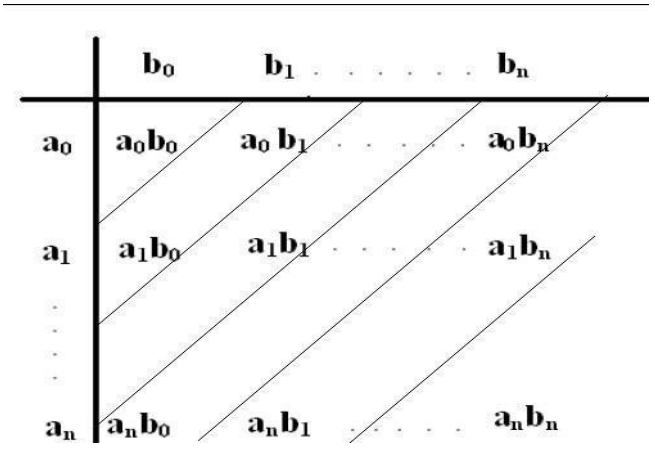

Figure 2:General diagram of n-point Linear Convolution

$$y(n) = \{a_0b_0, a_1b_0 + a_0b_1, a_2b_0 + a_1b_1 + a_0b_2, \ldots, a_nb_n\}$$

The partial (multiplication) results can be written in a matrix form to calculate the Convolution output.

Vedic Mathematics

Vedic Mathematics introduce the wonderful methods of Arithmetical computations, multiplications, algebraic operations, factorization and Geometry. 'Vedic Mathematics' is a tool based on 'Veda'. Veda is a Sanskrit word which means 'Knowledge'. It is very fast, efficient and easy to learn which found acceptance all over the world.

Vedic Suthras

Sri Bharati Krishna Tirtha Maharaja is introduced the Vedic maths algorithm from known

Vedas of Indian Sanskrit between the period of 1911-1918. Vedic Mathematics depends on 16 sutras[4], which are given in the table.

Multiplication techniques in Vedic Mathematics are

* Urdhava-Thiryagbhyam Suthra
* Nikhilam Suthra
* Ekadhikena Purvena

The most commonly used sutra is Urdhva Tiryagbhyam which gives an efficient multiplication. Different types of multipliers are there, like Array Multiplier, Wallace tree Multiplier and booth Multiplier, but the drawback of array and Wallace tree multiplier is they will just multiply the positive numbers, so to overcome this the booth multiplier is developed but the booth multiplier is applicable to small designs. To solve the above drawbacks the Vedic multiplier has been introduced. Vedic multiplier will multiply both positive and negative numbers.

Table 1: Suthras of Vedic Mathematics

No	Name	Explanation
1.	(Anurupye) Sunyamanyath	If one is in ratio other is zero
2.	Chalanakalanaabhyam	Difference and Similarities
3.	Ekadhikena Purvena	By one less than the previous one
4.	Chalanakalanaabhyam	Difference and Similarities
5.	Gunakasamuchyah	Factor of the sum is equal to the sum of the factors
6.	Gunitasamuchyah	The product of the sum is equal to the sum of the product
7.	Nikhilam Navatashcaramam Dashatah	All from 9 and last from 10
8.	Paraavartya Yojayet	Transpose and adjust
9.	Purna pooranaabhyam	By the completion or non-completion
10.	Sankalana-Vyavakalanabhyam	By addition and by Subtraction
11.	Shesanyankena Charamena	The reminders by the last digit
12.	Shunyam Saamyasamuchayet	When the sum is the same that sum is zero
13.	Sopaantyadvayamantyam	The ultimate and twice the penultimate
14.	Urdhavahiryagbhyam	Vertically and crosswise (criss-cross)
15.	Vyashti-Samashti	Part and Whole
16.	Yaavadunam	Whatever the extent of its deficiency

Urdhva Thiryagbhyam Method

Urdhva Tiryagbhyam is the most generalised sutra for implementation of Vedic multiplier designs. This method Tiryakbhyam Sutra is applicable to all cases of multiplication. This sutra performs the multiplication using the principle Vertically and crosswise multiplication. The generation of all partial products can be done with the concurrent addition of these partial products. The great advantage of this multiplier is gate delay and area increases very slowly

with the number of bits increases as compared to conventional multipliers. Hence it is more efficient than conventional multipliers. This architecture is quite efficient in terms of silicon area/speed.

(i) Two digit decimal multiplication

This is the general method of Multiplication in Vedic Maths. The example below, shows the two digit multiplication method.

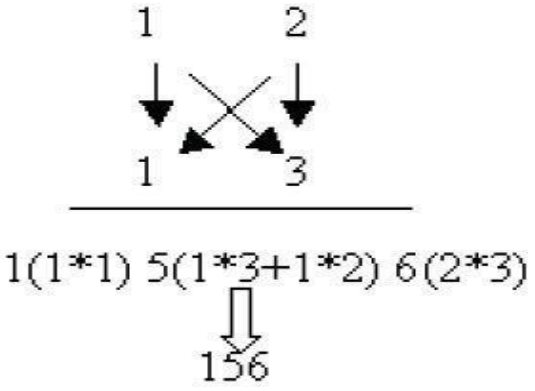

Figure 3: Two digit Multiplication

(ii) Three digit decimal multiplication

To illustrate the multiplication process, the multiplication of two decimal numbers (325 * 738)is explained here as line diagram. Multiplication proceeds from right to left, first digits are multiplied and added to the carry which is obtained from the previous step. This results in the generation of a part of the bits in the result. This process continues by adding the previous carry to the next step. When one or more lines are in one step then all the results are added. All the bits act as carry for the next step except, least significant bit which acts as the result bit. For the first time carry bit is zero.

The same method is used for the multiplication of any number of Digits.

(i) Binary (2X2) Vedic Multiplier

The Urdhva Tiryagbhyam sutra means the multiplication will be done in vertical and cross wise operation. Binary number multiplication is similar to the multiplication of decimal numbers. The 2 X 2 Vedic multiplier is multiplied in three steps.

Step 1: The first LSB of the two binary numbers to be multiplied vertically and these numbers are too added with the previous carry, in this case the previous carry is zero. In the output bits the LSB bit will be taken as a result and the remaining bits are forwarded to the next step.

Step 2: In this step the two binary bits can be multiplied cross wise and the produced results will be added to the previously generated carry and again, in the output bits the LSB bit will be taken as the result and the remaining bits are forwarded to the next step. .

Step 3: In this step the MSB bits to be multiplied vertically and the result of this is added to the previously generated carry and the output is taken as the result.

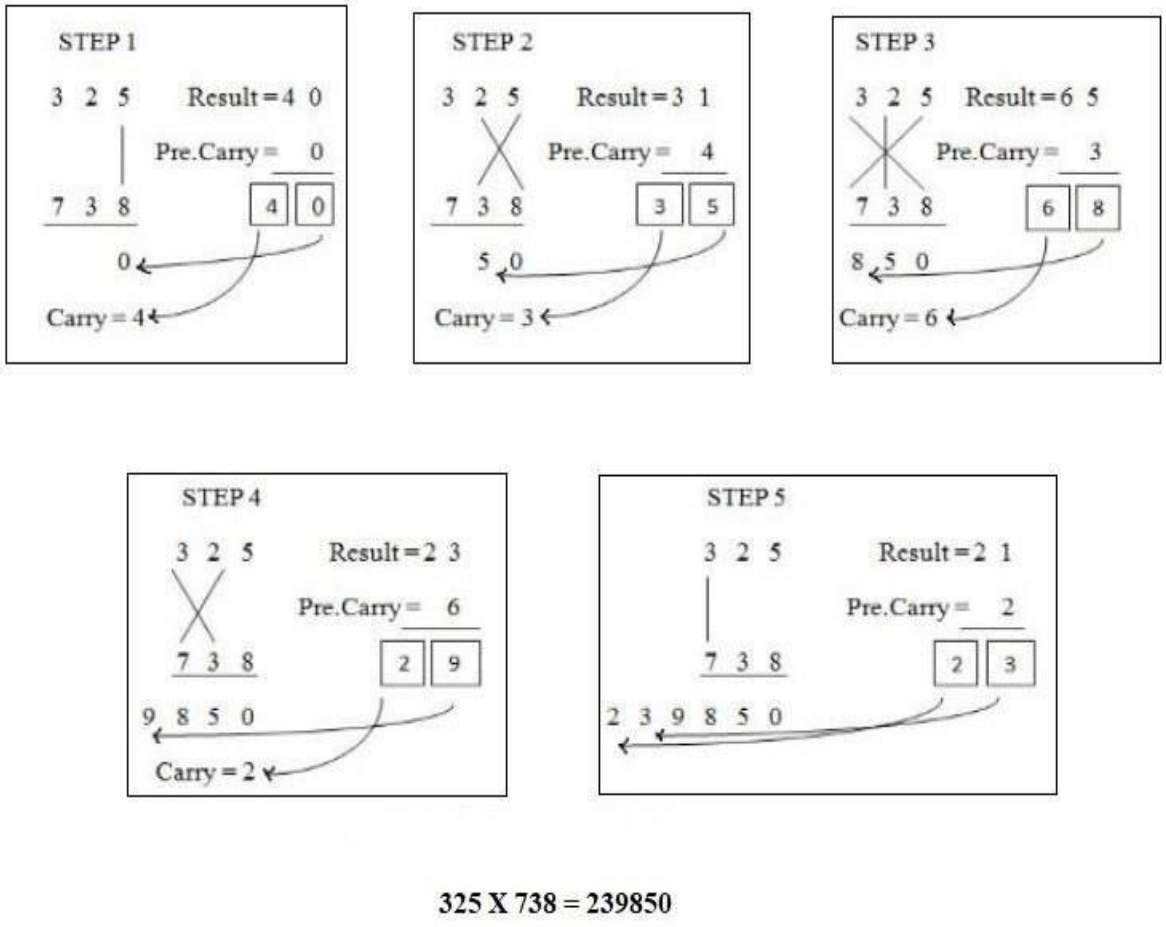

Figure 4: Three digit multiplication

The Vedic multiplication is shown in figure below.

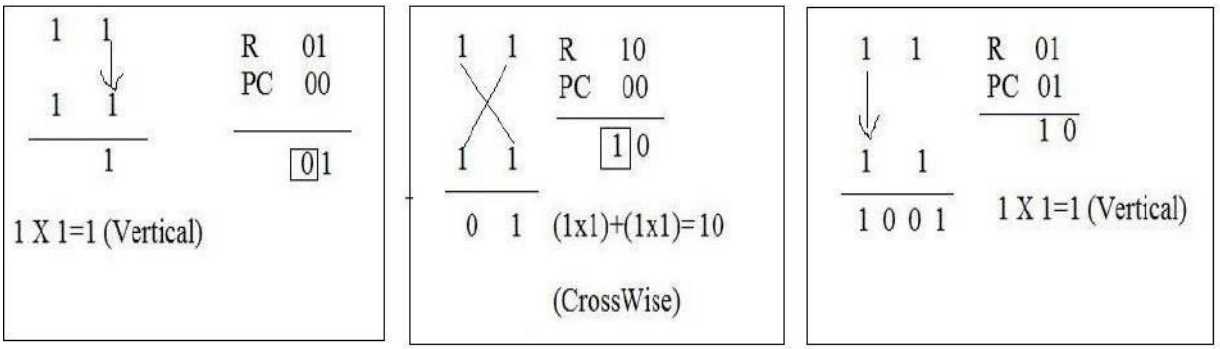

Figure 5: 2X2 Binary Multiplication - Vedic Method

Literature Survey

[1] S.Elango, P.Sampath, K. Shoukath Ali, Sajan P Philip Daniel Raj (2018) designed Linear Convolution using Vedic Multiplier. In their paper "Investigation and VLSI implementation of Linear Convolution Architecture for FPGA based Signal Processing Applications", they say

that, "as the number of bits increases, gate delay and area increases very slowly as compared to other conventional multipliers". They design 8-Bit and 16-Bit Vedic multiplier. They used Nine 8-Bit RCAs for 4X4 Multiplier. It is implemented in Xilinx Spartan 6. The comparison is done after implementing it in Spartan 6 and Altera Cyclone II.

[2] K Hari Kishore, Fazal Noorbasha, KattaSandeep, D. N. V. Bhupesh, SK. Khadar Imran, K. Sowmya (2018) Designed the basic building block of 4 bit Multiplier using "UrdhavThiryagb-hyam" algorithm, which is the general method of Multiplication in Vedic Mathematics. The paper "Linear convolution using UT Vedic multiplier" describes the properties of Convolution. Ripple Carry Adders are used for Addition in this paper. 4X4 Convolution is done using Six-teen 4X4 UT Multipliers, Six 8-bit RCAs and Three 9-bit RCAs. Propagation delay is reduced by half and power is also reduced considerably using Vedic multiplier.

[3] Neethu Johny and Mayur (2018) Designed Low power 4bit UT Vedic Multiplier. The8 bit multiplier is designed using the 4bit multiplier. Three different adders (Ripple Carry Adder, Carry Select Adder, MUX Adder)are used for the addition of Partial products and the performance is analyzed.

[4] Sheetal N Gadakh, AmitkumarKhade (2016) In paper "Design and Optimization of 16X 16 Bit Multiplier using Vedic Mathematics", done 16X16 bit multiplication using 8X8 Multiplier in FPGA platform. The paper explains the Sixteen 'Suthras' of Vedic Mathematics.

[5] Siba Kumar Panda, Ritisnigdha Das, S k SaifurRaheman, Tapasa RanjanSahoo(2015) Ex-plains the architecture of 4X4 Vedic Multiplier using RCA in "VLSI Implementation of Vedic Multiplier Using Urdhva-Tiryakbhyam Sutra in VHDL Environment: A Novelty". The architecture of 8X8 multiplier using 4X4 is also designed. This method is suggested for DSP processor to replace the traditional circuits. It is coded in VHDL and simulated using Xilinx ISE8.2 Software.

[6] Karnati Lavanya, VaddempudiKoteswaraRao (2015) Done Convolution and Deconvolution which include Multiplication and Division. VHDL implementation of Convolution using UT Multiplication and Nikhilam Division for FIR filter is used with Radix-256 Booth encoding. The circuit delay reduced by 18.27%. It is implemented using Xilinx ISE 13.1. Paper "A Novel VLSI Architecture for Convolution and Deconvolution using Higher Radix Algorithm"

[7] Aravind E Vijayan, Arlene John, Deepak Sen (2014) Performed 8-bit Vedic multiplier ar-chitecture which is suggested for Image Processing. In paper "Efficient Implementation of 8-bit Vedic Multipliers for Image Processing Application", the 4X4 Vedic Multiplier is implemented using 2X2 Multiplier as the basic building block. The system implemented on Xilinx Virtex4 based FPGA. Performance is evaluated using Xilinx ISim simulator. 1D and 2D convolution

and Cross convolution is performed.

[8] SavitaPatil, D.V. Manjunatha, DivyaKiran (2014) Done Multiplication with Array, using Nikhilam and UT based Multiplier in "Design of Speed and Power Efficient Multipliers Using Vedic Mathematics with VLSI Implementation". Power and Speed advantage is found more in Nikhilam Multiplier.

[9] Surabhi Jain, SandeepSaini (2014) Done convolution and Deconvolution of two finite length sequences in their paper "High Speed Convolution and Deconvolution Algorithm (Based on Ancient Indian Vedic Mathematics)". It is synthesized using Xilinx Design Suit 14.2, For Spartan3 and device XC3S400 5fg320. Circular convolution which is used in Electrical in DSP is also experimented.

[10] Sooraj N P (2014) in "Implementation of Unsigned Multiplier using modified CSLA" multiplied unsigned integers in which the portion of addition is improved. The Carry Select addition (CSLA) method is used and modified in a better way to improve the speed. The Modified Carry Select Adder (MCSLA) reduced the delay time in addition.

[11] Poornima M, Shivaraj Kumar Patil, Shivukumar, Shridhar K P, Sanjay H (2013) in "Implementation of Multiplier using Vedic Algorithm" used Vedic Multiplication algorithm for 2X2 Binary multiplication with two 'Half Adder' units. 4X4 multiplier is designed using 2X2 multiplier, so the delay in calculation of 'Carry' is avoided. The hierarchical multiplier design in this paper is claimed as a highly efficient method which gives the computational advantage offered by Vedic Method.

[12] Premananda B S, Samarth S Pai, Shashank B, Shashank S Bhatt (2013) in "Design and Implementation of 8-Bit Vedic Multiplier" extended the multiplication to 8X8, using 4X4 multiplier as the basic building block. Here partial products are calculated, so the number of steps required to calculate the final product will be reduced and hence there is a reduction in computational time. This increases the speed of the multiplier comparing with RCA method

[13] Hanumantharaju M.C, Jayalaxmi .H, Renuka R.K, Ravishankar .M (2007) Gone for "A High Speed Block Convolution using Ancient Indian Vedic Mathematics" High speed Block convolution in Overlap Add convolution method is done using VHDL coding for FPGA synthesis by Xilinx Spartan library.

[14] Akhalesh K Itawadia, Rajesh Mahle, Vivek Patel, Dandankumar (2013) in "Design a DSP operations using Vedic Mathematics" Used Vedic Method for Convolution in DSP operation, Linear and Circular Convolution is done âA˘ S¸ Cross correlation and Auto Correlation is experimented. It is simulated using MATLAB.

[15] YeshwantDeodhe, SandeepKakde, RushikeshDeshmukh(2013) Simulated their work in T-

Spice using 180nm CMOS technology and 75% power reduction achieved. Paper "Design and Implementation of 8-Bit Vedic Multiplier Using CMOS Logic"

[16] JubinHazra(2012)in "An Efficient Design Technique of Circular Convolution Circuit using Vedic Mathematics and McCMOS Technique", Designed Circular convolution using Vedic Mathematics in 45nm McCMOS technique and achieved 74-97% better performance.

Results

Output of 8 Bit - 4 Point Convolution

Convolution is implemented using 8X8 multiplier. In 8 bit convolution, the two set of input data contain four points (4 numbers), each number is of 8 bit. Sixteen 8X8 Multipliers are needed for 4 point - 8 bit Convolution. (Four 4X4 Multipliers are needed to construct one 8X8 Multipplier - So 64 units of 4X4 is needed to design the Convolution circuit). The result is a data set of 7 numbers (4+4-1), each number having 17 bit length.

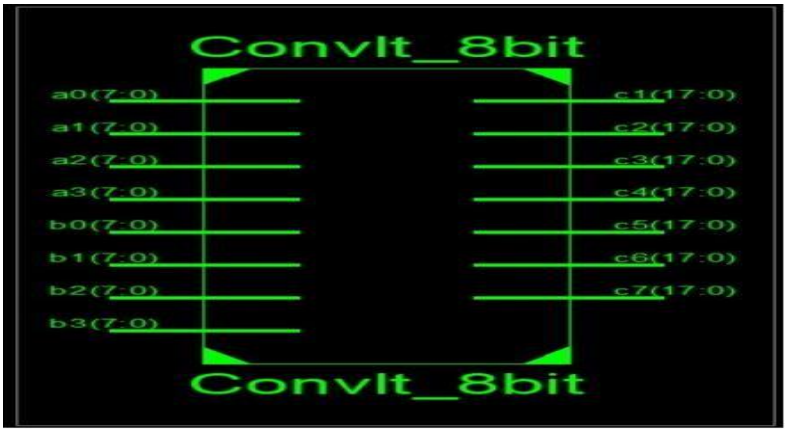

Figure 6: 8 Bit Convolution - RTL Diagram

The number of LUTs in Spartan-3 series is not sufficient for the convolution - so Spartan-6 is used.

Figure 7: 8 Bit Convolution - Simulation Output

Simulation output of the test data is -

{50,10,20,30} * {5,100,2,1} = {250,5050,1200,2220,3050,80}

{254,223,253,42} * {255,254,233,46} = {64770,121381,180339,138615,79875,21424,1932}

{20,35,1221,200}*{11,175,80,18} = {220,3885,9056,26535,45310,18178,3600}

Performance Comparisons

4X4 Vedic Multiplier

Different methods can be used to design the 4X4 Vedic multiplier and more than one ways to add the partial products. In paper [7], the 4X4 Multiplier is designed using 2X2 Vedic Multiplier, which is having minimum time delay. The chip area is minimum in Special Adder method. By comparing these, the "Special adder ” method is effective while considering the area usage and delay. In the given table, the performance of the Multiplier is compared in Spartan 3A.

Table 1: 4X4 Vedic Multiplier - Performance Comparison table

	Using 2X2	**LCA**	**Special Adder**
No. Of 4 Input LUTs	37/1408	41/1408	31/1408
No. Of Bonded IOBs	16/108	16/108	16/108
Time (ns)	11.839	14.384	11.960
Power (W)	0.010	0.010	0.010

16-bit Adder

The speed of the Multiplier is limited by the speed of the adders used in partial product addition. The architecture of the modified 16-bit CSLA using Binary to Exess-1 converter[10] for RCA to improve the speed, reduce the area and power is shown in Figure.

Table 2: 16 bit Adder - Performance Comparison table

	RCA	**LCA**	**MCSLA**
No. Of 4 Input LUTs	31/1408	32/1408	46/1408
No. Of Bonded IOBs	49/108	49/108	49/108
Time (ns)	19.740	19.515	14.472
Power (W)	0.010	0.010	0.010

Conclusion and Future Scope

This deals with the conclusion of the thesis work. It discusses the further improvements that can

be incorporated and the future scope of the thesis work. Vedic multiplier is superior in terms of speed and power consumption, when compared to the traditional method of multiplication. From various methods, the 'Special Adder' method is chosen to improve the performance. Hence, the architecture of linear convolution based on Vedic multiplier is used to enhance the speed of the system. The range of data is widened for eight bits. The Modified Carry Select Adder (MCSLA) method, which uses lesser area, is used to add the partial products and intermediate results. This also improves the system performance. The combination of low power and area efficient multiplier, makes this system a viable option. The system has been simulated for the hardware Xilinx Spartan 6 XC6SLX45-2CSG324 Field- Programmable Gate Array (FPGA). Even though, the system is faster comparing with other techniques for convolution, its data handling capacity is 8bit only. In future, the system can be extended to 16 bit or 32 bit without much coding complexity. The same 4X4 and 8X8 multipliers can be reused for it.

References

[1]**S.Elango, P.Sampath, K.Shoukath Ali, Sajan P Philip, A.Daniel Raj** Investigation and VLSI Implementation of Linear Convolution Architecture for FPGA based signal processing applications In International Journal of Pure and Applied Mathematics) Volume 119 No. 16 2018, Issue 1, PP 4607-4624.

[2]**K Hari Kishore, Fazal Noorbasha, Katta Sandeep, D N V Bhoopesh, S K Khadar Imran, K. Sowmya** Linear Convolution using UT Vedic Multiplier In International Journal of Engineering and Technology (2018), PP 409-412.

[3] **Neethu Johny, Mayur S M** Design and Implementation of a Low Power Vedic Multi-plier In International Journal for Research in Applied Science & Engineering Technology (IJRASET) Volume 6, Issue 4 (April 2018), PP 4156-4162.

[4] **Sheetal N Gadakh, Amitkumar Khade** Design and Optimization of 16X16 Bit Mul-tiplier using Vedic Mathematics In 2016 International Conference on Automatic Control and Dynamic Optimization Techniques (ICACDOT) pp 460-464.

[5] **Siba Kumar Panda, Ritisnigdha Das, S k Saifur Raheman, Tapasa Ranjan Sahoo** VLSI Implementation of Vedic Multiplier Using Urdhva Tiryakbhyam Sutra in VHDL Environment: A Novelty In IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 5, Issue 1, Ver. III (Jan - Feb. 2015), PP 17-24 .

[6] **Karnati Lavanya, Vaddempudi Koteswara Rao** A Novel VLSI Architecture for Convolution and Deconvolution using Higher Radix Algorithm In 2015 IEEE Power, Comm.n and Information Technology Conf. (PCITC) Siksha 'O' Anusandhan University, Bhubaneswar,

India.

[7] **Aravind E Vijayan, Arlene John, Deepak Sen** Efficient Implementation of 8-bit Vedic Multipliers for Image Processing Application In 2014 International Conference on Contemporary Computing and Informatics (IC3I) IEEE pp 544-552 .

[8] **Savita Patil, D V Manjunatha, Divya Kiran** Design of Speed and Power Efficient Multipliers using Vedic Mathematics with VLSI Implementation In 2015 International Conference on Advance Electronics, Computers and Communications(ICAECC), IEEE (2014)

[9] **Surabhi Jain, Sandeep Saini** High Speed Convolution and Deconvolution Algorithm (Based on Ancient Indian Vedic Mathematics) In 978-1-4799-2993-1/14/31.00 2014 IEEE

[10] **Sooraj N P** Implementation of Unsigned Multiplier using Modified CSLA In Emerging Trends in Electrical, Electronics & Instrumentation Engineering; An International Journal (EEIEJ) Volume 1, No.1, February 2014

[11] **Poornima M, Shivaraj Kumar Patil, Shivukumar, Shridhar K P, Sanjay H** Implementation of Multiplier using Vedic Algorithm In International Journal of Innovative Technology and Exploring Engineering(IJITEE) ISSN: 2278-3075, Volume 2, Issue 6, May 2013, PP 219-223.

[12] **Premananda S, Samarth S Pai, Shashank , Shashank S Bhatt** Design and Implementation of 8-Bit Vedic Multiplier In International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering Volume 2, Issue 12, December 2013, PP 5877-5882.

[13] **Hanumantharaju M.C, Jayalaxmi .H, Renuka R.K, Ravishankar .M** A High Speed Block Convolution using Ancient Indian Vedic Mathematics In International Conf. on Computational Intelligence and Multimedia Applications 2007 pp 169-174 .

[14] **Akhalesh K Itawadiya, Rajesh Mahle, Vivek Patel, Dadan Kumar** GDI Technique : Design a DSP operations using Vedic Mathematics In International conference on Communication and Signal Processing, April 3-5, 2013 IEEE pp 897-902 .

[15] **Yeshwant Deodhe, Sandeep Kakde, Rushikesh Deshmukh** Design and Implementation of 8-Bit Vedic Multiplier Using CMOS Logic In 2013 International Conference on Machine Intelligence Research and Advancement IEEE pp 340-344 .

[16] **Jubin Hazra** An Efficient Design Technique of Circular Convolution Circuit using Vedic Mathematics and McCMOS Technique In International Conference on Computer Communication and Informatics (ICCCI -2012), Jan. 10 - 12, 2012, Coimbatore, INDIA